Terasic TR4 FPGA Development Kit

1. Overview

The TR4 Development Board provides the ideal hardware platform for system designs that demand high-performance, serial connectivity, and advanced memory interfacing. Developed specifically to address the rapidly evolving requirements in many high end markets for greater bandwidth, improved jitter performance, and lower power consumption, the TR4 is powered by the Stratix® IV GX device and supported by industry-standard peripherals, connectors and interfaces that offer a rich set of features that is suitable for a wide range of compute-intensive applications.

The TR4 is supported by multiple reference designs and six High-Speed Mezzanine Card (HSMC) connectors that allow scaling and customization with mezzanine daughter cards. For

- **Company: Terasic**
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large-scale ASIC prototype development, multiple TR4s can be stacked together to create an easily-customizable multi-FPGA system.

2. Specification

FPGA Devices

Stratix IV GX EP4SGX230

- 228,000 logic elements (LEs)
- 17,133 total memory Kbits
- 1,288 18x18-bit multipliers blocks
- 2 PCI Express hard IP blocks
- 744 user I/Os
- 8 phase locked loops (PLLs)

Stratix IV GX EP4SGX530

- 531,200 logic elements (LEs)
- 27,376 total memory Kbits
- 1,024 18x18-bit multipliers blocks
- 4 PCI Express hard IP Blocks
- 744 user I/Os
- 8 phase locked loops (PLLs)

FPGA Configuration

- MAXII CPLD EPM2210 System Controller and Fast Passive Parallel (FPP) configuration
- On-board USB Blaster for use with the Quartus II Programmer
- Programmable PLL timing chip configured via MAX II CPLD
- Supports JTAG mode

Memory Devices

- 64MB Flash with a 16-bit data bus
- 2MB SSRAM (512K x 32)

DDR3 SO-DIMM Socket

- Up to 8GB capacity
- Maximum memory clock rate at 533MHz
- Theoretical bandwidth up to 68Gbps

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Buttons, Switches and LEDs

- 4 user-controllable LEDs
- 4 buttons for user-defined inputs
- 4 slide switches for user-defined inputs

On-Board Clocks

- 50MHz oscillator

SMA Connectors

- SMA connector pair for differential clock inputs
- SMA connector pair for differential clock outputs
- SMA connector for clock output
- SMA connector for external clock input

Two PCI Express x4 Connectors

- Support connection speed of Gen1 at 2.5Gbps/lane to Gen2 at 5.0Gbps/lane
- High-speed transceiver channels up to 6.5 Gbps
- Support downstream mode

Six 172-pins High Speed Mezzanine Card (HSMC)

- 6 HSMC connectors
- Configurable I/O standards - 1.5V, 1.8V, 2.5V, 3.0V
- Total of 16 high-speed transceivers up to 6.5 Gbps
- Among HSMC Port A to D, there are 55 true LVDS TX channels to 1.6Gbps and 17 emulated LVDS TX channels up to 1.1Gbps
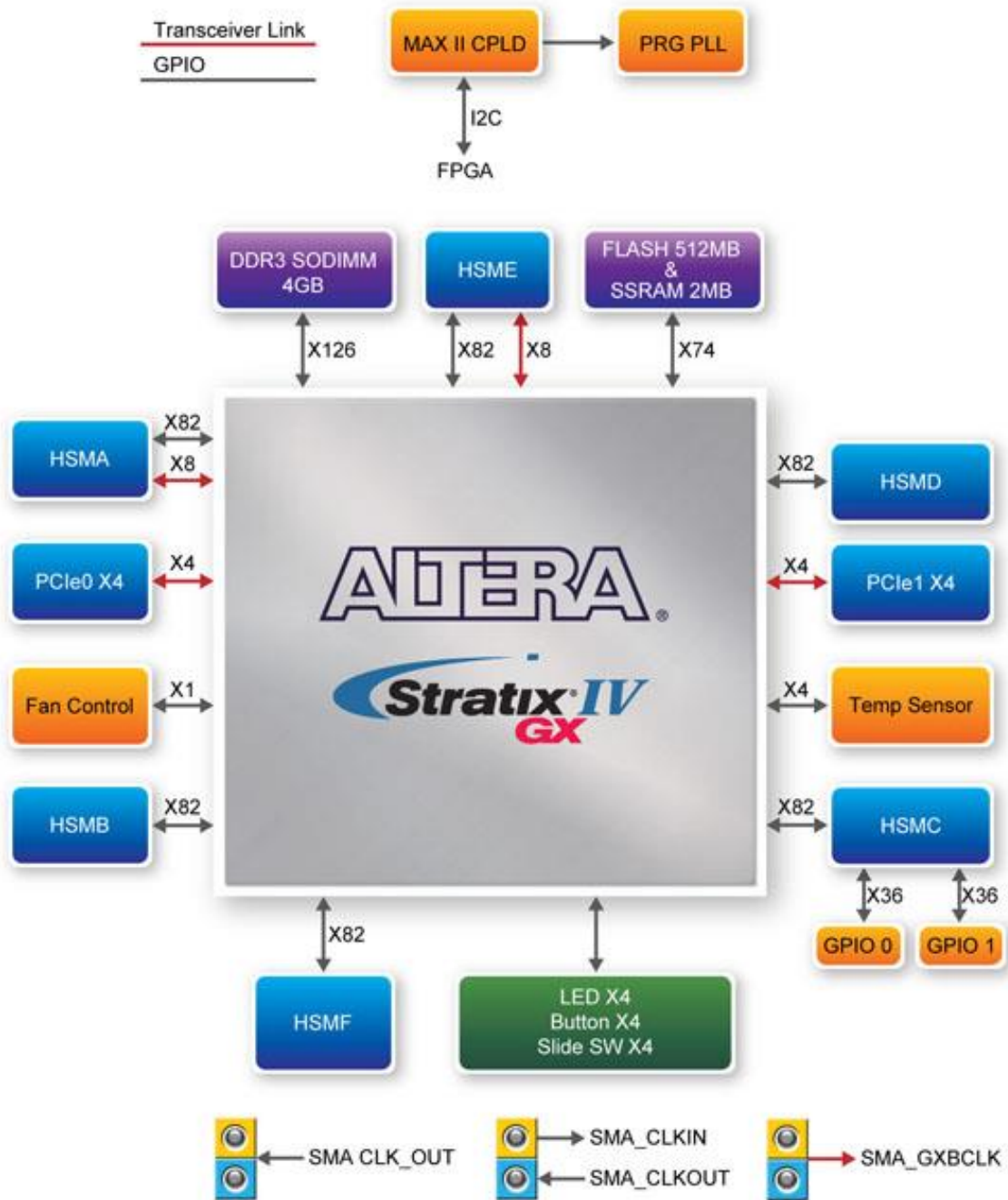
Two 40-pin Expansion Headers

- 72 FPGA I/O pins; 4 power and ground lines
- Configurable I/O standards - 1.5V, 1.8V, 2.5V, 3.0V
- Shares pins with HSMC Port
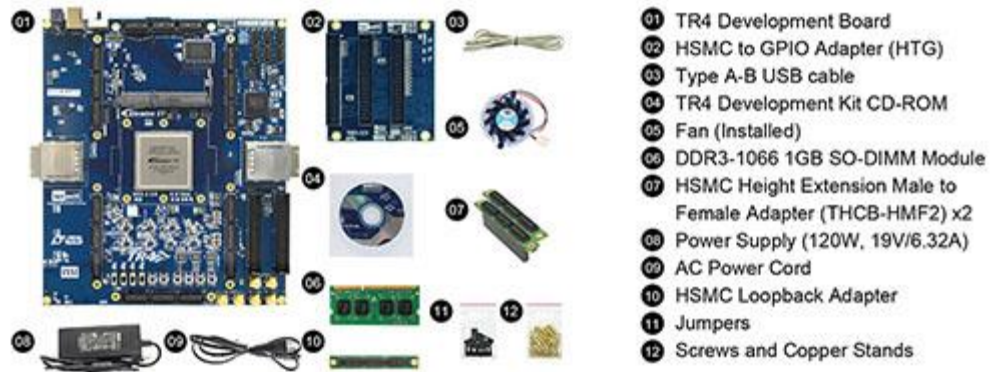
Power

- Standalone DC 19V input

Block Diagram

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3. Kit content

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The TR4 package includes:

01 TR4 Development Board
02 HSMC to GPIO Adapter (HTG)
03 Type A-B USB cable
04 TR4 Development Kit CD-ROM
05 Fan (Installed)
06 DDR3-1066 1GB SO-DIMM Module
07 HSMC Height Extension Male to
   Female Adapter (THCB-HMF2) x2
08 Power Supply (120W, 19V/6.32A)
09 AC Power Cord
10 HSMC Loopback Adapter
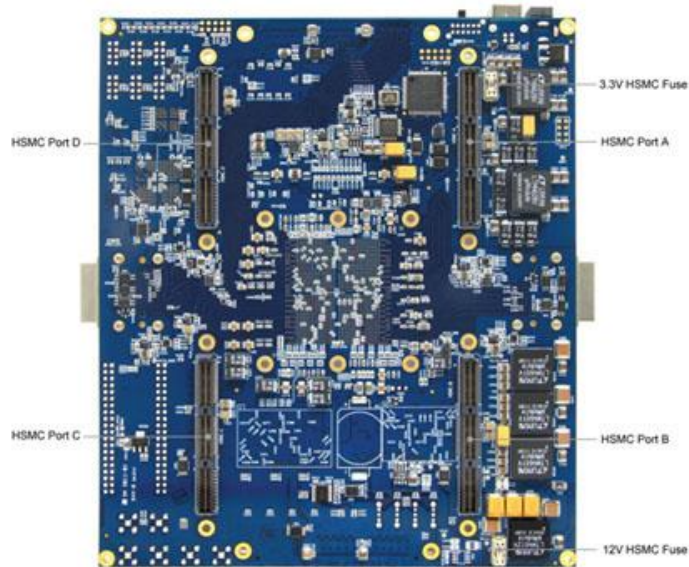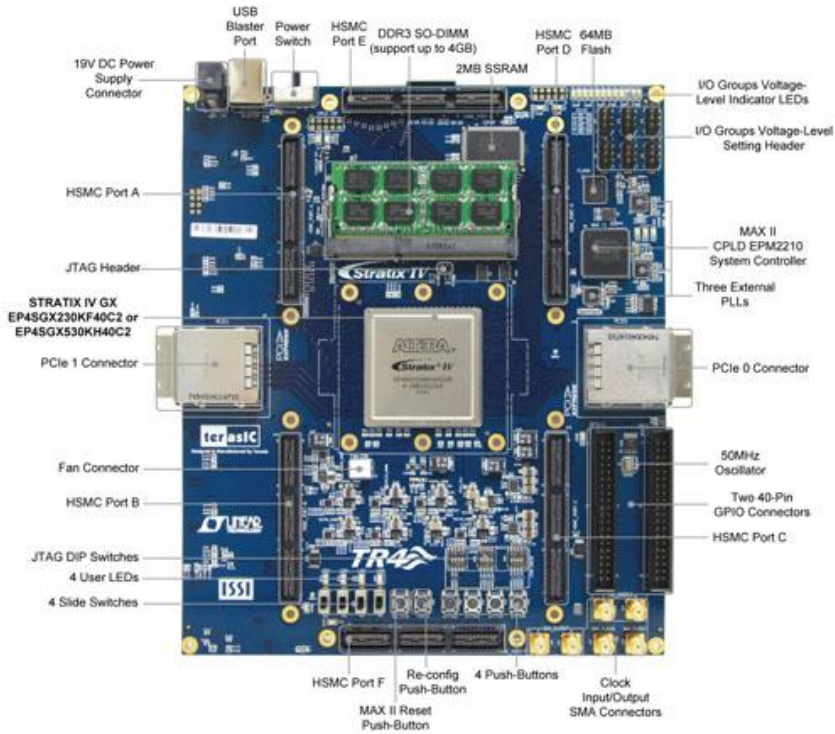11 Jumpers
12 Screws and Copper Stands

- Quartus design software license is not included in this kit.

4. Layout

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- Size：182.36 x 210.82 mm

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