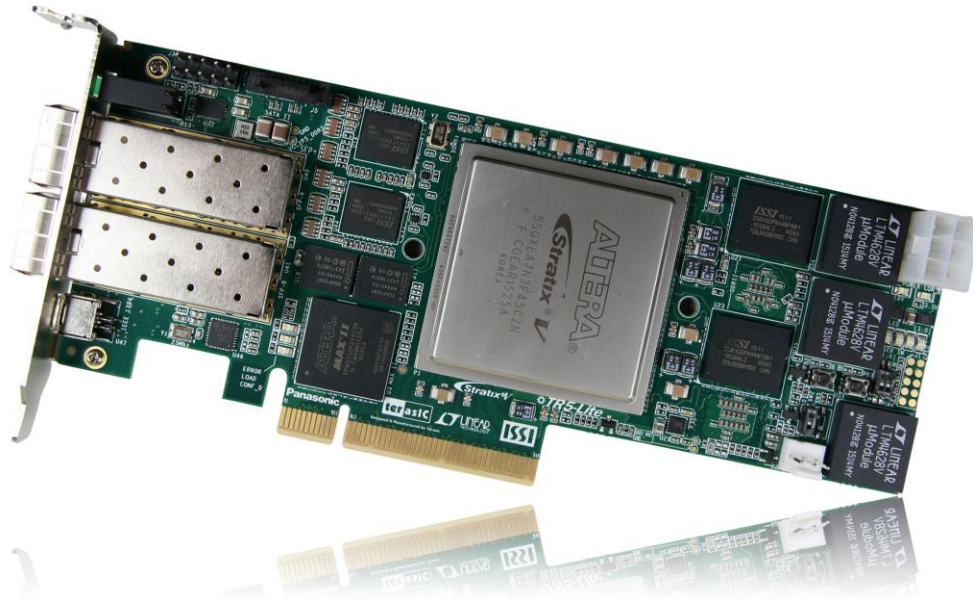


TR5-Lite

1. Overview



The TR5-Lite Stratix V FPGA Development Kit is a slim form-factor PCIe board that features maximum power in a minimum size. Perfect for 1U chassis servers and other stringent environments, the TR5-Lite includes high speed SFP+ interfaces and high-bandwidth memory architecture for high performance computing, cloud systems, and ultra low-latency trading.

2. Specification

Altera Stratix® V GX FPGA (5SGXEA7N2F45C2)

- JTAG header for FPGA programming
- Fast passive parallel (FPPx32) configuration via MAX II CPLD and flash memory

General user input / output:

- 4 LEDs
 - 1 LED Array
 - 2 push-buttons
 - 2-position DIP switch
-
- **Company: Terasic**
 - **Tel: +886-3-5750880**
 - **Fax: +886-3-5726690**
 - **Add: 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan**

On-Board Clock

- 50MHz Oscillator
- Programmable oscillators Si570 and CDCM61004

Memory

- 36MB 550MHZ ISSI
- 2GB 933MHz DDR3 SDRAM
- 256MB FLASH

Communication Ports

- Two SFP+ connectors
- One Serial ATA (SATA II) host port
- PCI Express (PCIe) x8 edge connector
- One RS422 transceiver with 1394 connector

System Monitor and Control

- Temperature sensor
- Fan control

Power

- PCI Express 6-pin power connector, 12V DC Input
- PCI Express edge connector power

Mechanical Specification

- PCI Express low-profile and half-length

Connectivity

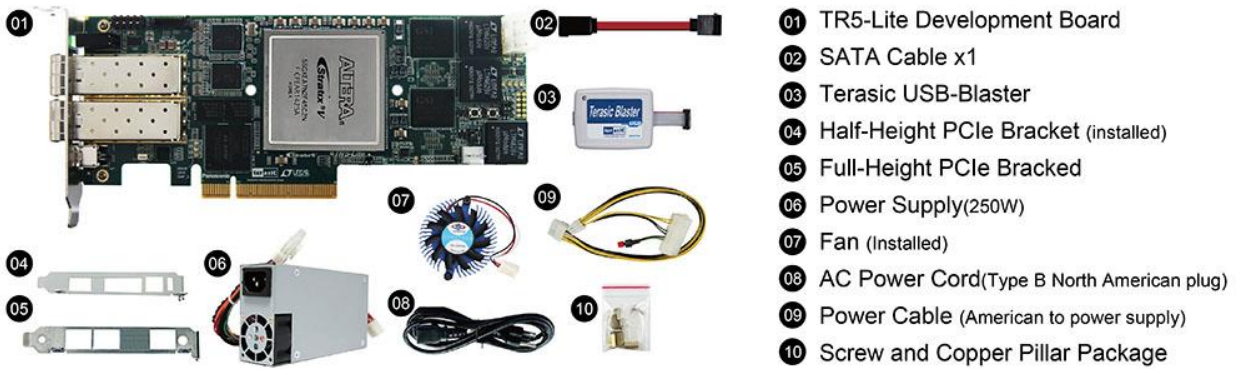
Demonstration

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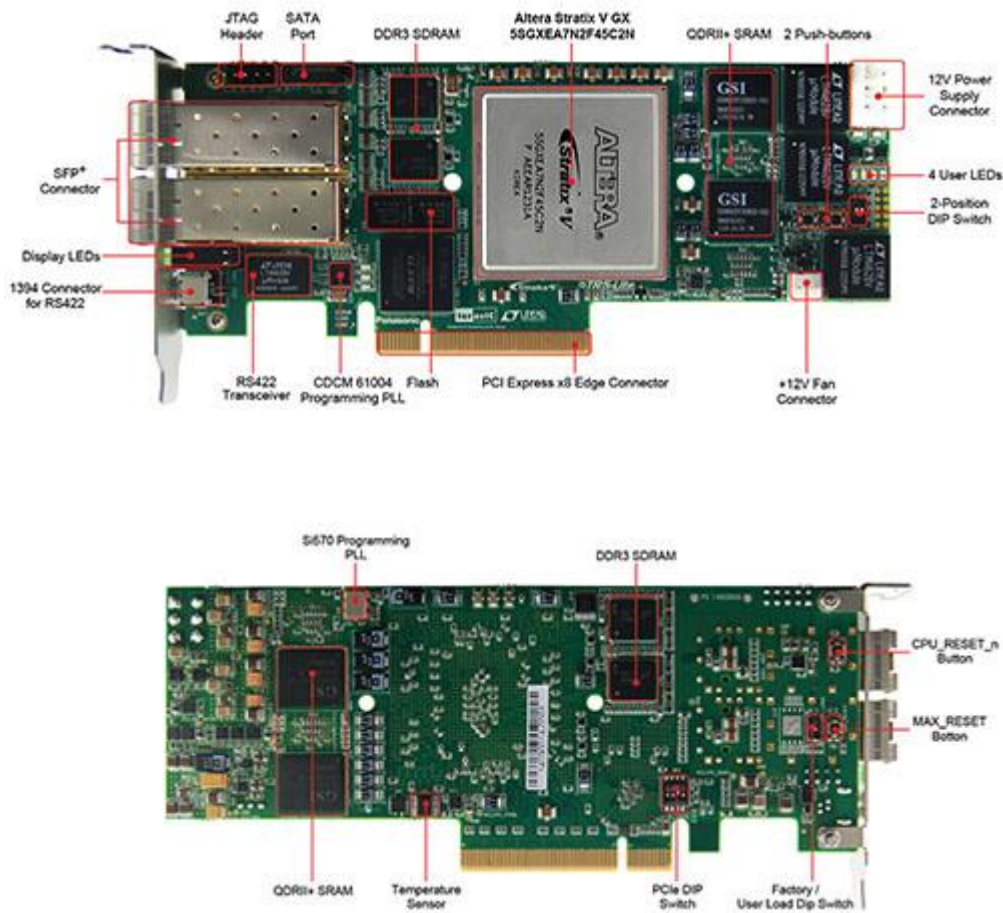


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3. Kit content



4. Layout



- Size : 64.4 * 167.6 mm

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